PROCESS FOR ETCHING SILICON WAFERS

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application Serial No. 60/411,544, filed September 18, 2002, and U.S. Provisional Application Serial No. 60/487,662, filed July 16, 2003, the entire disclosures of which are hereby incorporated by reference.

FIELD OF THE INVENTION

[0002] The present invention relates generally to a process for etching a silicon wafer with a caustic etchant. The present invention further relates to a process for etching a silicon wafer to produce silicon wafers with improved surface characteristics such as flatness and nanotopography.

BACKGROUND OF THE INVENTION

[0003] Silicon wafers are typically obtained by a multi-step process, including: slicing a single crystal silicon ingot in a direction normal to the axis of the ingot to produce thin wafers; chamfering or profiling the edges of the wafers; grinding or lapping the wafers to remove surface damage caused by the slicing process; chemically etching the wafers to remove mechanical damage produced by the prior shaping steps; and finally, chemically/mechanically polishing the edge, and at least one surface of each wafer with, for example, a colloidal silica slurry and a chemical etchant, to ensure that the wafers have highly flat, reflective and damage-free surfaces. The wafers are then typically cleaned and quality inspected prior to being packaged.

[0004] Prior to chemical etching, silicon wafers typically exhibit surface and/or subsurface defects such as embedded particles and physical damage such as micro-cracks, fractures or stress imparted to the wafer by processes such as lapping, grinding and edge profiling. These defects generally occur in the region extending from the surface of the wafer to at least about 2.5 μm or

greater below the surface of the wafer. To remove these defects, therefore, at least about 2.5 μm of silicon is typically removed from the surface of the wafer using an acidic and/or caustic chemical etchant, thus removing the embedded particles, contaminants, and physical damage contained in the removed layer of silicon.

[0005] Both acidic and caustic chemical etchant formulations are utilized in etching the surface of a silicon wafer. One of the most common acidic etchant formulations comprises a solution of hydrofluoric acid (HF), nitric acid (HNO_3), and water. Caustic etchants typically comprise one or more alkaline hydroxides, such as potassium hydroxide (KOH) or sodium hydroxide (NaOH), and water.

[0006] Acidic etchants are preferred in some instances because they yield a smooth wafer surface generally exhibiting less surface roughness than wafers etched with a caustic etchant. However, acidic etchants are prone to the formation of unwanted gas-phase and solid-phase chemical species on the etched surface of the wafer, creating stains that inhibit further reaction and produce inconsistent etching results (See, e.g., D.G. Schimmel et al., "An Examination of the Chemical Staining of Silicon", J. Electrochem. Soc., Vol. 125, p. 152-155 (1978)). The acidic etchants containing nitric acid react during the etching process to produce toxic gases containing oxides of nitrogen (NO_x), necessitating the use of safety controls since these gases are toxic to the human body and special disposal procedures to avoid polluting the environment and to comply with environmental regulatory requirements. Also, in order to obtain a sufficiently smooth surface using acidic etchants, a relatively large amount of silicon must be removed from the wafer surfaces, typically about 10-15 μm from the front and back surface of the wafer. Generally speaking, limiting the amount of silicon removed from the wafer surfaces is preferred in order to limit the variation in wafer thickness.

[0007] Acidic etchants generally etch the wafer at a high etch rate and the etching rate is controlled primarily by the mass transfer of the reactants to the wafer surface. Due to the difficulty in accurately controlling the removal of silicon during a mass transfer dominated etching process, the flatness of an acid etched wafer is subject to degradation. Also, rapid, mass transfer dominated acid etching processes, in conjunction with bubble masking (i.e., gaseous etching reaction byproducts such as hydrogen and NO_x adhered to portions of the wafer surface), tend to introduce a significant variation in the nanotopography of the etched wafer. (See, e.g., Kulkarni et al., "Acid-Based Etching of Silicon Wafers: Mass-Transfer and Kinetic Effects", J. Electrochem. Soc., Vol. 147 (1), pp. 176-188 (2000)).

[0008] Caustic etchants offer several advantages over acidic etchants. For example, caustic etchants tend to produce wafers having flatter surfaces than wafers etched with acidic etchants, even while using relatively simple etching equipment. In general, caustic etchants etch more slowly than acidic etchants and the etching process is controlled primarily by the reaction kinetics rather than the mass transfer of the reactants to the wafer surface. Limiting the amount of silicon removed from the surface during chemical etching is desired in order to limit the variation in wafer thickness, or, flatness. The Global Backside-referenced Indicated Range (GBIR), the difference between the maximum and minimum thickness of the wafer, typically increases as the amount of silicon removed from the wafer surfaces increases. Caustic etchants typically yield wafers having a low GBIR (e.g., of about +0.1 μm), whereas acidic etchants typically yield wafers having a high GBIR (e.g., ranging from about +0.5 to +1.5 μm). In this respect, caustic etching solutions are preferred because the amount of silicon that must be removed from the wafer surfaces during subsequent processing to achieve satisfactory GBIR is much less as compared to acid etched

wafers. Moreover, the reduction in the etch reaction rate with caustic etchants tends to reduce the density of gaseous byproduct-containing bubbles adhered to the surface of the wafer. The reduced amount of gas bubbles present on the surface of the wafer in turn reduces the effect of "bubble masking" on the nanotopography of the wafer. Therefore, even though gas bubbles may be formed on the surface of the wafer, because the process is controlled by reaction kinetics, the nanotopography of a caustic etched wafer is typically more consistent than that of an acid etched wafer.

[0009] In addition to providing etched wafers with improved surface characteristics such as flatness and nanotopography, caustic etching processes are inherently safer and can be operated at lower cost than acid etching processes. Any gaseous byproducts from the caustic etching process are typically generated in a sufficiently low quantity such that they may be disposed of in a safe and simple manner. For example, any hydrogen generated is typically in a quantity below its lower explosive limit, thus allowing for safe and simple disposal. Caustic etchants tend to react with skin tissue less quickly than acidic etchants, making accidental exposure to caustic etchants less dangerous to operating personnel than acidic etchants.

[00010] However, caustic etchants are not superior to acidic etchants in every respect. As mentioned previously, acid etched wafers exhibit less surface roughness than caustic etched wafers. Generally, acid etching produces wafers with an average surface roughness (Ra) of from about 0.09 μm to about 0.16 μm while caustic etching generally produces wafers with an average surface roughness of from about 0.27 μm to about 0.35 μm Ra. The greater degree of roughness for caustic etched wafers is due in large part to preferential etching along crystallographic planes which produces a faceted surface characterized by a "scale-like" appearance.

[00011] The increased surface roughness and faceting caused by conventional caustic etchants can be overcome by subsequent polishing, but the time required to polish the front surface and edge surface of the wafer increases significantly as surface roughness increases. Thus, as compared to acid-etched wafers, the increased surface roughness and faceting of caustic etched wafers reduces the throughput and increases the cost of the overall manufacturing process. Additionally, the increased surface roughness is sometimes so great that device manufacturers which specify that the backside surface of the wafer remain "as etched" find caustic etched wafers unacceptable because they require further processing of the backside before the wafer is suitable for use.

[00012] Accordingly, a need continues to exist for a caustic etching process capable of producing wafers readily processed to exhibit desired standard surface characteristics.

SUMMARY OF THE INVENTION

[00013] Among the objects of the invention, therefore, is the provision of an improved caustic etchant for removing silicon from the surface of a silicon wafer; the provision of a process for etching silicon wafers with a caustic etchant to produce etched wafers having improved flatness and nanotopography as compared to wafers etched with acidic etchants; the provision of a process for etching silicon wafers with a caustic etchant to produce etched wafers having improved surface characteristics as compared to wafers etched with conventional caustic etchants; the provision of a process for etching silicon wafers with a caustic etchant to produce etched wafers having decreased surface roughness as compared to wafers etched with conventional caustic etchants; the provision of a process for caustic etching of silicon wafers which improves the throughput of subsequent polishing steps; the provision of a process for etching silicon wafers with enhanced safety characteristics as compared to processes

for etching silicon wafers using acidic etchants; and the provision of a caustic etchant and a process for etching silicon wafers which reduces the amount of toxic emissions and/or the cost of environmental controls.

[00014] Briefly, therefore, the present invention is directed to an etching process for removing silicon from the surface of a silicon wafer which comprises contacting the surface of the silicon wafer with a caustic etchant in the form of an aqueous solution comprising water and a source of hydroxide ions. The concentration of water in the caustic etchant is less than 45% by weight.

[00015] In another embodiment, the concentration of the source of hydroxide ions in the caustic etchant contacted with the surface of the silicon wafer is greater than 55% by weight.

[00016] In a further embodiment, the concentration of the source of hydroxide ions in the caustic etchant contacted with the surface of the silicon wafer is at least about 70% of the saturation concentration of the source of hydroxide ions in the caustic etchant.

[00017] In a still further embodiment, the etching process for removing silicon from the surface of a silicon wafer comprises contacting the surface of the silicon wafer with a caustic etchant in the form of an aqueous solution comprising water, hydroxide ions, and a salt additive that does not decompose or react in the caustic etchant. The salt additive comprises a compound selected from the group consisting of inorganic alkali and alkaline earth metal salts and mixtures thereof and the concentration of the salt additive in the caustic etchant is at least about 4 mole percent.

[00018] In yet a still further embodiment, the etching process for removing silicon from the surface of a silicon wafer comprises contacting the surface of the silicon wafer with a caustic etchant in the form of an aqueous solution comprising water, hydroxide ions, and a salt additive comprising a compound selected from the group

consisting of potassium carbonate and potassium fluoride. The concentration of the salt additive in the caustic etchant is at least about 1 mole percent.

[00019] The invention is further directed to a caustic etchant for etching a silicon wafer which comprises an aqueous solution comprising water, hydroxide ions, and a salt additive that does not decompose or react in the caustic etchant. The salt additive comprises a compound selected from the group consisting of inorganic alkali and alkaline earth metal salts and mixtures thereof and the concentration of salt additive in the caustic etchant is at least about 4 mole percent.

[00020] In another embodiment, the caustic etchant for etching a silicon wafer comprises an aqueous solution comprising water, hydroxide ions, and a salt additive comprising a compound selected from the group consisting of potassium carbonate and potassium fluoride. The concentration of salt additive in the caustic etchant is at least about 1 mole percent.

[00021] The invention is further directed to a single crystal silicon wafer comprising a central axis, a front surface and a back surface which are generally perpendicular to the central axis, a peripheral edge, and a radius, R, extending from the central axis to the peripheral edge of the wafer. After polishing, the single crystal silicon wafer exhibits a front surface site flatness average of less than about 0.13 μm, a front surface site flatness maximum of less than about 0.18 μm, a front surface 2 mm x 2 mm nanotopography of less than about 20 nm, and a front surface 10 mm x 10 mm nanotopography of less than about 40 nm.

[00022] Other objects and features of this invention will be in part apparent and in part pointed out hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

[00023] Fig. 1 is a photomicrograph, produced using an Olympus, BH3 microscope at 200X magnification showing

the surface of a P^+ silicon wafer etched in a caustic liquid etchant system in accordance with the present invention as described in Example 1.

[00024] Fig. 2 is a photomicrograph, produced using an Olympus, BH3 microscope at 200X magnification showing the surface of a P^+ silicon wafer etched in a caustic liquid etchant system in accordance with the present invention as described in Example 1.

[00025] Fig. 3 shows the gloss measurements of the 360 P^+ wafers etched in accordance with the present invention as described in Example 1.

[00026] Fig. 4 shows the overall flatness, or, GBIR values for the P^- wafers etched as described in Example 2, before and after etching.

[00027] Fig. 5 shows the maximum site flatness least squares range (SFQRmax) values for the P^- wafers etched as described in Example 2, before and after etching.

[00028] Fig. 6 shows the gloss and average surface roughness (μm Ra) measurements for the P^- wafers etched as described in Example 2 after etching.

[00029] Fig. 7 shows the etching rates for the P^- wafers etched as described in Example 3 over the course of 83 etching runs.

[00030] Fig. 8 shows the overall flatness, or, GBIR values for the P^- wafers etched as described in Example 3, after lapping and after etching.

[00031] Fig. 9 shows SFQRmax values for the P^- wafers etched as described in Example 3, after lapping and after etching.

[00032] Fig. 10 is a photomicrograph, produced using an Olympus, BH3 microscope at 200X magnification showing the surface of a P^- silicon wafer from Group 1 of the wafers etched in accordance with the present invention as described in Example 3. The wafer shown in Fig. 10 was etched during etching run 23.

[00033] Fig. 11 is a photomicrograph, produced using an Olympus, BH3 microscope at 200X magnification showing

the surface of a P^- silicon wafer from Group 1 of the wafers etched in accordance with the present invention as described in Example 3. The wafer shown in Fig. 11 was etched during etching run 50.

[00034] Fig. 12 is a photomicrograph, produced using an Olympus, BH3 microscope at 200X magnification showing the surface of a P^- silicon wafer from Group 1 etched in accordance with the present invention as described in Example 3. The wafer shown in Fig. 12 was etched during etching run 70.

[00035] Fig. 13 is a photomicrograph, produced using an Olympus, BH3 microscope at 200X magnification showing the surface of a P^- silicon wafer from Group 2 etched in accordance with the present invention as described in Example 3.

[00036] Fig. 14 shows SFQRmax values for the P^+ silicon wafers etched as described in Example 4 using a caustic etchant containing approximately 58% by weight sodium hydroxide. The SFQRmax values are shown for the wafer after lapping and before etching, after etching, and after buffing.

[00037] Fig. 15 shows SFQRmax values for the P^+ silicon wafers etched as described in Example 4 using a caustic etchant containing approximately 45% by weight potassium hydroxide. The SFQRmax values are shown for the wafer after lapping and before etching, after etching, and after buffing.

[00038] Fig. 16 shows SFQRmax values before and after polishing of the P^+ silicon wafers etched as described in Example 4 using both an etchant containing approximately 58% by weight sodium hydroxide and an etchant containing approximately 45% by weight potassium hydroxide.

[00039] Fig. 17 shows all-site SFQR values before and after polishing of the P^+ silicon wafers etched as described in Example 4 using both an etchant containing approximately 58% by weight sodium hydroxide and an etchant containing approximately 45% by weight potassium hydroxide.

[00040] Fig. 18 shows all-site SFQR values for P^+ silicon wafers etched in accordance with the standard acidic etching protocol set forth in U.S. Patent No. 5,340,437 described in Example 4.

[00041] Fig. 19 is a photomicrograph, produced using an Olympus, BH3 microscope at 1000X magnification showing the surface of a wafer sample etched in accordance with Example 5.

[00042] Fig. 20 is a photomicrograph, produced using an Olympus, BH3 microscope at 200X magnification showing the surface of a wafer sample etched in accordance with Example 6.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[00043] A caustic etching process which produces silicon wafers with improved surface characteristics has been discovered. The process of the present invention provides the commonly recognized benefits of caustic etching while overcoming or minimizing the commonly recognized limitations of conventional caustic etching and acid etching. Wafers etched in accordance with the present invention exhibit a decreased surface roughness compared to wafers etched with a conventional caustic etchant while also exhibiting a high degree of flatness and low variation in nanotopography after polishing as compared to acid etched wafers. Wafers etched in accordance with the present invention may further exhibit a high degree of flatness and low variation in nanotopography after polishing as compared to wafers etched with conventional caustic etchants. The caustic etchant utilized in the present invention is in the form of an aqueous solution comprising water and a source of hydroxide ions. In one embodiment, the caustic etchant is generally characterized as having a lower concentration of water than previously employed. In another embodiment, the caustic etchant may additionally or alternatively be characterized as containing a higher concentration of the source of hydroxide ions than previously employed. In a still

further embodiment, the caustic etchant includes a salt additive.

[00044] The process of the present invention employs as a starting material a silicon wafer which has been sliced from a single crystal silicon ingot and further processed, for example, using conventional grinding apparatus to profile or chamfer the peripheral edge of the wafer. Such processing reduces the risk of wafer damage during further processing, reduces the non-uniform damage caused by the slicing process and roughly improves the general flatness and parallelism of the front and back surfaces. The wafer may be sliced from the ingot using any means known to persons skilled in the art, such as, for example, an internal diameter slicing apparatus or a wiresaw slicing apparatus. Grinding processes are well known to persons skilled in the art. Typical grinding processes generally remove about 20 μm to about 30 μm of stock from each surface of the wafer to roughly improve flatness using, for example, a resin bond, 1200 to 6000 mesh wheel operating at about 2000 RPM to about 4000 RPM.

[00045] Either as an alternative or in addition to grinding, the wafers may be lapped using a planetary lapper such as the AC 1200, AC 1400, AC 1500 lappers manufactured by Peter Wolters AG (Rendsburg, Germany), or lappers manufactured by SpeedFam KK (Japan) or Fujikoshi (Japan). A suitable lapping grit is an Al_2O_3 abrasive, such as FO-1200, PWA 9, or PWA 11M manufactured by Fujimi America, Inc. (Wilsonville, OR). If the wafers are lapped in addition to grinding, the order of these mechanical shaping processes is not critical.

[00046] The silicon wafer may have any conductivity type, resistivity, diameter and target thickness appropriate for the intended semiconductor application. For example, the diameter is generally at least about 100 mm and typically is 150 mm, 200 mm, 300 mm or greater and the thickness may be from about 475 μm to about 900 μm or greater, with the thickness typically increasing with

increasing diameter. The wafer may also have any crystal orientation. In general, however, the wafers may have <100> and <111> crystal orientations.

[00047] Having been sliced from the ingot and subjected to the mechanical shaping processes described above, the wafer typically exhibits surface and/or subsurface defects such as embedded particles and physical damage such as micro-cracks, fractures or stress. These defects generally occur in the region extending from the surface of the wafer to at least about 2.5 μm or greater below the surface of the wafer. In addition, the surface of the wafer generally has an average surface roughness of at least about 50 nm to about 200 nm Ra or greater. The surface roughness may be measured using any metrology device capable of measuring the surface roughness. Such devices are well known in the art. For example, the surface roughness may be measured using an MP 3000 surface measurement device commercially available from Chapman Instruments (Rochester, NY) or other metrology devices such as an AFM microscope, a Nomarski microscope at 50X magnification, a Wyko-2D microscope equipped with a 10X magnification, an optical interferometer or a Federal Products Surface Analyzer 5000 manufactured by the former Federal Products, Inc., now known as Mahr Federal, Inc. (Providence, RI).

[00048] The shaped wafer is then subjected to chemical etching to substantially reduce these mechanical defects. In accordance with the present invention, a caustic etchant in the form of an aqueous solution comprising water and a source of hydroxide ions is employed. As described in greater detail below, the caustic etchant may further include a salt additive. Although the etching process of the present invention may consist only of etching using the caustic etchants described herein, it should be understood that the caustic etchant disclosed herein may be utilized in multi-step

etching protocols in which acidic etchants and/or other caustic etchants are also employed.

[00049] In accordance with one embodiment of the present invention, the concentration of water in the aqueous caustic etchant solution is lower than conventional caustic etchants. More particularly, the concentration of water in the caustic etchant is less than 45% by weight water. Experimental evidence to date indicates that a wafer etched with the caustic etchant of the present invention has a decreased surface roughness compared to that of a wafer etched with a conventional caustic etchant and improved flatness and nanotopography as compared to both wafers etched with acidic etchants and wafers etched with conventional caustic etchants. The improved surface characteristics are believed to be due, at least in part, to the increase in surface tension of the caustic etchant when the concentration of water in the caustic etchant is less than 45% by weight. This increase in surface tension decreases the average size of gas bubbles present on the wafer surface during the etching process. Since it is believed that facet size is at least in part determined by the size of gas bubbles on the wafer surface, this reduction in the size of bubbles on the wafer surface results in decreased bubble masking and allows for more uniform etching of the wafer surface. The more uniform etching of the wafer surface is also believed to be due, at least in part, to the reduced contact angle of the smaller bubbles with the wafer surface observed when the surface tension of the etchant is increased. The smaller contact angle reduces the amount of wafer surface in direct contact with each individual bubble, providing a more uniform etched wafer surface.

[00050] It is further believed that the improved surface characteristics of the etched wafers are due in part to a reduction in the oxidation rate during the etching process as the concentration of water in the caustic etchant decreases. The etching of silicon proceeds

by virtue of a two-step process: silicon oxidation by the water present in the etchant to produce silicon dioxide and dissolution of the silicon dioxide by the alkali component of the source of hydroxide ions present in the etchant. Thus, the reduction in water concentration will decrease the oxidation rate and, in turn, decrease the etch rate.

[00051] The improved surface characteristics attributed to a reduction in the overall oxidation rate may more particularly be due to a decrease in preferential etching along the <100> crystallographic planes of the wafer. Specifically, a decrease in the etching rate along the <100> crystallographic planes of up to 40 percent has been observed. The effect of the decreased etch rate is more pronounced along the <100> crystallographic planes since the etch rate along these planes is greater than that along all other planes. Since the difference between the etch rate along the <100> wafer surfaces and all other wafer surfaces is diminished, the faceting and the roughness associated therewith are likewise decreased. Generally, the ratio of the etch rate along the <100> crystallographic planes to all other wafer surfaces will be from about 0.7 to about 5. In accordance with the present invention, the ratio of the etch rate along the <100> crystallographic planes to all other wafer surfaces is preferably near 1.

[00052] Typically the caustic etchant comprises at least about 10% by weight water, more typically at least about 20% by weight water and, still more typically, at least about 25% by weight water. Preferably, the caustic etchant comprises from about 25% to about 45% by weight water, more preferably from about 30% to about 42% by weight water and, still more preferably, from about 30% to about 37% by weight water.

[00053] In certain instances it may be useful to define the concentration of water in the caustic etchant in terms of mole percent. Thus, generally water is present in the caustic etchant at a concentration of no more than

about 68 mole percent. Typically, water is present in the caustic etchant at a concentration of no more than about 65 mole percent, more typically at a concentration of no more than about 55 mole percent and, still more typically, at a concentration of no more than about 45 mole percent. Preferably, the water is present in the caustic etchant at a concentration of from about 5 to about 45 mole percent and, more preferably, from about 5 to about 20 mole percent.

[00054] The desired lower water concentration may be provided by increasing the concentration of the source of hydroxide ions present in the caustic etchant.

[00055] In accordance with one embodiment of the present invention, the concentration of the source of hydroxide ions in the caustic etchant is greater than 55% by weight. Preferably, the concentration of the source of hydroxide ions in the caustic etchant is at least about 57% by weight, more preferably at least about 58% by weight, even more preferably at least about 60% by weight and still more preferably at least about 62% by weight. In accordance with one embodiment, the concentration of the source of hydroxide ions in the caustic etchant is at least about 65% by weight. Typically, the concentration of the source of hydroxide ions in the caustic etchant is no more than about 75% by weight. Thus, the concentration of the source of hydroxide ions in the caustic etchant is typically from about 58% by weight to about 70% by weight, preferably from about 58% to about 65% by weight and, more preferably, from about 62% by weight to about 65% by weight. Suitable sources of hydroxide ions include tetramethyl ammonium hydroxide and alkali metal hydroxides such as sodium hydroxide, potassium hydroxide, cesium hydroxide and lithium hydroxide and mixtures thereof. In a preferred embodiment, the source of hydroxide ions comprises potassium hydroxide and, in another preferred embodiment, comprises sodium hydroxide.

[00056] It has been observed that the decrease in facet size and surface roughness due to reduced bubble size and increased surface tension observed with a caustic etchant having a reduced water concentration is more pronounced when using sodium hydroxide as the source of hydroxide ions. Thus, in a preferred embodiment, the source of hydroxide ions comprises sodium hydroxide. In an embodiment wherein the source of hydroxide ions comprises sodium hydroxide, the concentration of sodium hydroxide in the caustic etchant is preferably at least about 58% by weight, more preferably at least about 61% by weight and even more preferably at least about 62% by weight. Typically, the concentration of sodium hydroxide is no more than about 68% by weight. Thus, the concentration of sodium hydroxide in the caustic etchant is typically from about 58% to about 68% by weight, preferably from about 58% to about 63% by weight, and more preferably from about 61% to about 63% by weight. Although sodium hydroxide is a preferred source of hydroxide ions, it should be understood that a caustic etchant utilizing other hydroxide ion sources (e.g., potassium hydroxide) at concentrations in excess of 55% by weight also provides the advantageous results discussed herein. In an embodiment wherein the source of hydroxide ions comprises potassium hydroxide, the concentration of potassium hydroxide in the caustic etchant is preferably at least about 57% by weight and more preferably at least about 60% by weight. Typically, the concentration of potassium hydroxide is no more than about 63% by weight. Thus, the concentration of potassium hydroxide in the caustic etchant is typically from about 57% to about 63% by weight and preferably from about 60% to about 63% by weight.

[00057] In certain instances (e.g., when components of the caustic etchant have widely varying molecular weights as in the case of a caustic etchant including a salt additive) it may be useful to define the concentration of the source of hydroxide ions in the caustic etchant in

terms of mole percent. Thus, generally the source of hydroxide ions is present in the caustic etchant at a concentration of no more than about 70 mole percent. Typically, the source of hydroxide ions is present in the caustic etchant at a concentration of no more than about 68 mole percent, more typically no more than about 55 mole percent and, still more typically, no more than about 45 mole percent. Typically, the source of hydroxide ions is present in the caustic etchant at a concentration of from about 30 to about 45 mole percent. In the case of a caustic etchant wherein the source of hydroxide ions comprises sodium hydroxide, the concentration of sodium hydroxide in the caustic etchant is typically no more than about 55 mole percent. Typically, in such an embodiment, the concentration of sodium hydroxide in the caustic etchant is at least about 35 mole percent and, more typically, from about 40 to about 50 mole percent. Further in accordance with such an embodiment, water is typically present in the caustic etchant at a concentration of no more than about 68 mole percent. When the source of hydroxide ions comprises potassium hydroxide, the concentration of potassium hydroxide in the caustic etchant is typically no more than about 55 mole percent. Typically, in such an embodiment, the concentration of potassium hydroxide in the caustic etchant is at least about 30 mole percent and, more typically, from about 30 to about 40 mole percent. Further in accordance with such an embodiment, water is typically present in the caustic etchant at a concentration of no more than about 68 mole percent.

[00058] In accordance with a preferred embodiment of the present invention, the concentration of the source of hydroxide ions in the caustic etchant is at or near the saturation point at the prescribed etching temperature. As the temperature of the caustic etchant increases, the concentration of the source of hydroxide ions in the caustic etchant can generally be increased. However, it

should be understood that the concentration of the source of hydroxide ions in the caustic etchant preferably is not increased to a point such that undesired precipitates form. That is, it is preferred that the caustic etchant comprising water and a source of hydroxide ions, as well as any other components, be prepared such that the etchant comprises a homogenous single liquid phase mixture at the prescribed etching temperature wherein all the components are miscible. Precipitate formation is preferably avoided since any precipitates formed may attach to or form on the surface of the wafer, thereby interfering with the etching process and adversely affecting the nanotopography of the etched wafer. The presence of precipitates in the caustic etchant may also cause operational issues such as clogging of process equipment or interfering with control of the temperature of the etchant.

[00059] In one embodiment of the present invention, the concentration of the source of hydroxide ions in the caustic etchant is defined as being at least about 70% of the saturation concentration of the source of hydroxide ions in the caustic etchant at the prescribed etching temperature, more preferably at least about 74% and, still more preferably, at least about 77%. However, in order to reduce the risk of precipitate formation, the concentration of the source of hydroxide ions in the caustic etchant is generally no more than about 95% of the saturation concentration of the source of hydroxide ions in the caustic etchant. Thus, typically, the concentration of the source of hydroxide ions in the caustic etchant is from about 70% to about 95% of the saturation concentration of the source of hydroxide ions in the caustic etchant at the prescribed etching temperature. In a preferred embodiment, the concentration of the source of hydroxide ions in the caustic etchant is from about 74% to about 90% of the saturation concentration of the source of hydroxide ions in the caustic etchant at the prescribed etching temperature. In another preferred embodiment of the present invention,

the concentration of the source of hydroxide ions in the caustic etchant is from about 74% to about 81% of the saturation concentration of the source of hydroxide ions in the caustic etchant at the prescribed etching temperature.

[00060] In the practice of the present invention, the temperature of the caustic etchant is typically maintained at a temperature of at least about 70°C, more typically at least about 75°C and, still more typically, at least about 80°C. In one embodiment of the present invention, the temperature of the caustic etchant is maintained at a temperature of at least about 90°C and, in another embodiment, at a temperature of at least about 100°C. The temperature of the caustic etchant is typically maintained from about 70°C to about 120°C, preferably from about 70°C to about 110°C, more preferably from about 70°C to about 100°C, still more preferably from about 75°C to about 90°C, and, even more preferably, from about 75°C to about 85°C. When the caustic etchant comprises a salt additive, higher temperatures within the ranges set forth above (e.g., temperatures from about 100°C to about 120°C) may be utilized to promote dissolution of the salt additive in the caustic etchant. However, it should be understood that the preferences set forth above apply generally regardless of whether the caustic etchant includes a salt additive.

[00061] As mentioned, the caustic etchant used in the practice of the present invention may comprise a salt additive which contributes to improved surface characteristics of the etched wafer. It should be understood that in the practice of the present invention in which a salt additive is included in the caustic etchant, it is not necessary that the etchant contain a low concentration of water and/or high concentration of a source of hydroxide ions as described herein. However, including a salt additive in a caustic etchant exhibiting either or both of these characteristics is contemplated in the present invention. Thus, in one embodiment in which a salt additive is included in the etchant, the concentration

of the source of hydroxide ions in the etchant is at least about 55% by weight.

[00062] The salt additive is selected such that it does not decompose nor react to any appreciable extent with the other components of the caustic etchant (e.g., the source of hydroxide ions). That is, the salt additive is not irreversibly changed when mixed with water and the source of hydroxide ions in the caustic etchant. However, it should be understood that decomposition does not include dissolution such that it is acceptable in the practice of the present invention that the salt additive dissociate into its respective anion and cation when mixed with the other components of the caustic etchant.

[00063] The salt additive included in the caustic etchant is suitably selected from inorganic alkali metal and alkaline earth metal salts, their hydrates, and mixtures thereof that are soluble in the caustic etchant at the desired concentration and temperature. Generally, suitable inorganic salts include alkali and/or alkaline earth metal salts selected from the group consisting of lithium, sodium, potassium, rubidium, cesium, francium, beryllium, magnesium, calcium, strontium, barium and radium salts and mixtures thereof. Preferably, the inorganic salt is a potassium salt or a sodium salt, with potassium salts being especially preferred. Suitable potassium salt additives for use in the practice of the present invention include potassium carbonate, potassium phosphate, potassium fluoride, potassium iodide, potassium chloride, potassium pyrophosphate, potassium subphosphate, potassium hypophosphate, potassium orthophosphite, potassium nitrate, potassium nitrite, potassium peroxycarbonate, potassium chlorate, potassium acetate, potassium citrate, potassium borate, potassium fluoroborate, potassium sulfate, potassium propionate, potassium selenate, potassium stannate, potassium tartrate, potassium thioantimonate, potassium thiocyanate, potassium thiosulfate, potassium tungstate and mixtures thereof. Suitable sodium salt

additives for use in the practice of the present invention include sodium carbonate, sodium phosphate, sodium fluoride, sodium iodide, sodium chloride, sodium pyrophosphate, sodium subphosphate, sodium hypophosphate, sodium orthophosphite, sodium nitrate, sodium nitrite, sodium peroxycarbonate, sodium chlorate, sodium acetate, sodium citrate, sodium borate, sodium fluoroborate, sodium sulfate, sodium sulfide, sodium propionate, sodium selenate, sodium stannate, sodium tartrate, sodium thioantimonate, sodium thiocyanate, sodium thiosulfate, sodium tungstate and mixtures thereof. In addition, suitable salt additives include magnesium sulfate and magnesium hydroxide.

[00064] In a preferred embodiment, the inorganic salt additive comprises a potassium halide salt (e.g., potassium fluoride, potassium iodide and/or potassium chloride) and/or potassium carbonate. In an especially preferred embodiment, the salt additive is potassium fluoride and, in another, potassium carbonate.

[00065] Any salt additive included in the caustic etchant may also be a hydrate of any of the aforementioned inorganic salts (e.g., potassium fluoride hydrate ($KF_2 \cdot H_2O$)).

[00066] The concentration of the salt additive in the caustic etchant is somewhat dependent upon the solubility of the additive in the other components of the etchant solution at the prescribed etching temperature. Generally, any beneficial effects of including a salt additive in the caustic etchant are improved as the concentration increases. However, the quantity of salt additive included in the caustic etchant preferably does not exceed the solubility limit such that the presence of undissolved solids in the etchant is avoided.

[00067] The concentration of the salt additive in the caustic etchant will typically be no more than about 25% by weight. Generally, the concentration of the salt additive is at least about 5% and, more typically at least about 10%

by weight. Thus, the concentration of the salt additive is typically from about 5% to about 25% by weight and, more typically, from about 10% to about 25% by weight. In the case of a salt additive comprising either potassium fluoride or potassium carbonate, the concentration of salt additive in the caustic etchant will typically be no more than about 25% by weight and, more typically, from about 5% to about 25% by weight. Since the molecular weights of suitable salt additives may vary widely, it is useful to characterize the concentration of the salt additive in the caustic etchant in terms of mole percent. Preferably, the concentration of the salt additive in the caustic etchant is at least about 1 mole percent, more preferably at least about 4 mole percent, still more preferably at least about 5 mole percent and, even more preferably, at least about 10 mole percent. Typically, the concentration of the salt additive in the caustic etchant is from about 4 to about 15 mole percent, more typically from about 5 to about 15 mole percent and, still more typically, from about 10 to about 15 mole percent. In the case of potassium halide salts, the concentration of the salt additive in the caustic etchant is preferably at least about 1 mole percent, more preferably at least about 4 mole percent, still more preferably at least about 5 mole percent, and, even more preferably, at least about 10 mole percent. Typically, in the case of potassium halide salts, the concentration of the salt additive in the caustic etchant is from about 1 to about 15 mole percent, preferably from about 5 to about 15 mole percent and more preferably from about 10 to about 15 mole percent. In a preferred embodiment, the concentration of the potassium halide salt in the caustic etchant is from about 10 to about 12 mole percent. In the case of potassium carbonate or potassium fluoride, the concentration of the salt additive in the caustic etchant is preferably at least about 1 mole percent and more preferably at least about 3 mole percent. Typically, in the case of potassium carbonate or potassium fluoride the

concentration of the salt additive in the caustic etchant is from about 1 to about 6 mole percent and preferably from about 3 to about 6 mole percent.

[00068] Preferably, any salt additive added to the caustic etchant will be added to the other components of the caustic etchant (e.g., the mixture of water and the source of hydroxide ions) as a concentrated salt additive solution. The preferred solvent for a salt additive solution is water. Preferably, the components of the caustic etchant are selected such that the etchant comprises a homogeneous, single liquid phase mixture wherein all the components are miscible.

[00069] In one preferred embodiment in which the caustic etchant includes a salt additive, the source of hydroxide ions is sodium hydroxide and, in another, potassium hydroxide. In an especially preferred embodiment in which the caustic etchant includes a salt additive, the source of hydroxide ions is potassium hydroxide. Potassium hydroxide is an especially preferred source of hydroxide ions when a salt additive is included in the caustic etchant because it is believed that potassium hydroxide results in reduced impurities being present on the wafer surface.

[00070] In an embodiment in which the caustic etchant comprises a salt additive, the etchant is characterized by the concentration of hydroxide ions present in the etchant rather than the concentration of the source of the hydroxide ions. In such an embodiment, the concentration of hydroxide ions in the caustic etchant is preferably no more than about 20 mole percent and more preferably no more than about 15 mole percent. Typically, the concentration of hydroxide ions in the etchant is from about 5 to about 15 mole percent and more typically from about 10 to about 15 mole percent. In a preferred embodiment, the concentration of hydroxide ions in the etchant is from about 10 to about 12 mole percent.

[00071] In an embodiment in which the caustic etchant includes a salt additive, the concentration of water in the etchant is preferably no more than about 85 mole percent. Typically, the water concentration in the etchant is from about 70 to about 85 mole percent and more typically from about 75 to about 85 mole percent.

[00072] Overall, when the caustic etchant includes a salt additive, the components of the caustic etchant are selected such that its pH is preferably at least about 13 and more preferably from about 13.9 to about 14.

[00073] The purity of the source of hydroxide ions, water, and any salt additive included in the caustic etchant, should be at least sufficient for general silicon wafer processing. In particular, it is preferred that the caustic etchant exhibit a low concentration (e.g., less than 5 parts per billion (ppb)) of contaminants, in particular, nickel, copper, and iron, to prevent contamination of the wafer surface. Thus, preferably, the source of hydroxide ions and any salt additive each comply with the purity profiles as set forth in the Semiconductor Equipment and Materials International (SEMI) standards and preferably contain no more than about 5 ppb of any of these contaminants.

[00074] Silicon wafers ready to be etched are immersed in the caustic etchant either individually or multiple wafers are immersed concurrently. Suitable immersion etchers include those commercially available from SPEC (Valencia, California), Toho (Japan) and Dan Science (Japan). Although the precise number of wafers etched at a time is not narrowly critical, typically 25 or more wafers are etched at a time. Conventionally, the wafers are held in a cassette which is placed in a rotatable basket and the basket is rotated while immersed in the etchant. The rate of rotation of the wafers held in the basket is also not narrowly critical, however, any rotation of the wafer should be sufficient to maintain sufficient agitation of the etchant bath and a substantially uniform etchant

temperature. Generally, agitation contributes to a uniform etchant temperature. While the etchant is heated to a suitable temperature, the etchant is likewise cooled by conduction and/or convection due to contact of the etchant with the walls of the etch tank. Agitation mixes the portions of the etchant having varied temperatures and, thus, provides a more uniform temperature throughout the etchant in contact with the wafer surface. Typically, the rate of rotation varies from about 1 revolution per minute to about 100 revolutions per minute. Preferably, the rate of rotation is from about 1 revolution per minute to about 45 revolutions per minute and, more preferably, from about 5 revolutions per minute to about 30 revolutions per minute.

[00075] Generally, the residence time of the caustic etchant contacting the wafer in the etch tank (i.e., the ratio of the volumetric capacity of the etch tank to the flow rate of the etchant) is at least about 2 minutes. Typically, the residence time of the caustic etchant in the etch tank is from about 2 minutes to about 24 minutes, more typically from about 2 minutes to about 12 minutes and, still more typically, from about 2 minutes to about 4 minutes.

[00076] The amount of time the wafer remains in contact with the caustic etchant is generally determined based on the desired amount of silicon to be removed from the surface of the wafer. The amount of silicon to be removed is a function of the thickness of the damage layer, mechanical damage imparted to the wafer during slicing, grinding and/or lapping process steps, the depth at which the defects occur beneath the surface of the wafer, and the desired characteristics of the finished wafer. Generally, at least about 10 μm of stock is removed in terms of total thickness from both the front and back surface of the wafer. Typically, from about 10 μm to about 30 μm of stock is removed in terms of total thickness of both sides of the wafer, more typically, from about 15 μm to about 25 μm and,

still more typically, from about 17 μm to about 23 μm. In view of the foregoing, the surface of the wafer typically remains in contact with the caustic etchant for at least 5 minutes. Typically, the surface of the wafer remains in contact with the caustic etchant for from about 5 minutes to about 15 minutes, preferably for from about 9 minutes to about 11 minutes, and, more preferably, for from about 10 minutes to about 10.5 minutes until the desired amount of stock is removed from the wafer.

[00077] The amount of stock actually removed can be determined by measuring the total thickness of the wafer prior to and after etching. Once the amount of stock removed is determined for a given wafer, contact time, etchant concentration and conditions, the time a subsequent wafer remains immersed may be varied to increase or decrease the amount of stock removed. Alternatively, the concentration of the etchant may be monitored wherein the reduction in the concentration of the source of hydroxide ions in the etchant is directly related to the amount of material removed from the wafer surface. Accordingly, the reduction in the concentration of the source of hydroxide ions in the etchant may be monitored and used to predict the amount of stock removed. The etchant concentration may be measured by any means known to persons skilled in the art, and may be determined by, for example, flow-injection analysis by measuring the pH, conductivity, or ionic strength of a diluted portion of the etchant and also by ion chromatography of a diluted portion of the etchant. The etchant concentration may also be determined by inductively coupled plasma magnetic spectroscopy of a diluted portion of the etchant. Persons skilled in the art may recognize and utilize other methods for determining the amount of stock removed without departing from the scope of the present invention (e.g., measuring the weight of the wafer before and after etching).

[00078] In addition to contacting the surface of the wafer to be etched with the etchant by immersion, it should

be understood that the surface of the wafer to be etched may also be contacted with the caustic etchant by other suitable means such as by spin etching. In spin etching, the backside surface of the wafer is placed on a rotatable chuck, and the caustic etchant is sprayed on the opposite surface while the wafer is rotated at high speed. While not critically narrow, the rotation rate of the wafer during spin etching is typically greater than in immersion etching and preferably is at least about 50 revolutions per minute, more preferably at least about 150 revolutions per minute and, still more preferably, at least about 250 revolutions per minute. Typically, the rate of rotation of the wafer during spin etching ranges from about 50 revolutions per minute to about 650 revolutions per minute and, more typically, from about 150 revolutions per minute to about 550 rotations per minute. Suitable spin etchers include those commercially available from SEZ (Villach, Austria). During spin etching, the rotatable chuck may be heated to maintain a uniform temperature throughout the surface of the wafer.

[00079] Regardless of the manner by which the surface of the wafer is contacted with the caustic etchant, the etchant may be reused to subsequently etch additional wafers. Accordingly, additional quantities of water, source of hydroxide ions and/or salt additive may be added to the caustic etchant to replace the portion of the etchant that is consumed or otherwise lost during the etching of previous wafers.

[00080] The wafer etched in accordance with the present invention is removed from the etchant and rinsed with deionized water. Alternatively, other rinsing solutions known in the art may be used in place of the deionized water including, for example, dilute (e.g., less than 3% by weight) hydrogen peroxide, and ozonated deionized water. Other solutions, for example, SC1, a standard cleaning solution of ammonium hydroxide, hydrogen

peroxide, and water may be used in place of deionized water.

[00081] The wafer etched in accordance with the present invention exhibits advantageous surface characteristics, including improved surface roughness, as compared to wafers etched with conventional caustic etchants, and improved flatness and nanotopography after polishing, as compared to acid etched wafers. Wafers etched in accordance with the present invention may further exhibit improved flatness and nanotopography as compared to wafers etched with conventional caustic etchants after polishing.

[00082] In accordance with an embodiment of the present invention in which the source of hydroxide ions is present in the caustic etchant at a concentration of greater than 55% by weight, the etched wafer typically exhibits an average surface roughness of less than about 0.19 μm Ra. Preferably the wafer etched in accordance with such an embodiment exhibits an average surface roughness of from about 0.12 μm to about 0.19 μm Ra. Wafers etched using a caustic etchant containing one of the salt additives discussed above typically exhibit an average surface roughness of from about 0.14 μm and about 0.36 μm Ra which is closer to the desired roughness of an acid-etched wafer (typically from about 0.09 μm to about 0.16 μm Ra) and can be easily processed to the desired roughness (e.g., by buffing and/or polishing). By way of comparison, a wafer etched using a caustic etchant that does not comprise a source of hydroxide ions present at a concentration of greater than 55% by weight or a salt additive typically has an average surface roughness of about 0.27 μm to about 0.35 μm Ra.

[00083] Wafers etched in accordance with the present invention generally exhibit an overall flatness (i.e., Global Backside-referenced Indicated Range or GBIR) of no greater than about 0.8 μm. Typically, a wafer etched using an etchant in which the source of hydroxide ions is present

at a concentration of greater than 55% by weight exhibits a GBIR of from about 0.2 μm to about 0.8 μm. Typically, a wafer etched using a caustic etchant containing one of the salt additives discussed above exhibits a GBIR of less than about 0.7 μm, and more preferably less than about 0.5 μm.

[00084] Generally, wafers etched in accordance with the present invention exhibit improved front surface nanotopography. Typically, acid etched wafers exhibit a front surface 2 mm x 2 mm nanotopography of at least about 75 nm and a front surface 10 mm x 10 mm nanotopography of at least about 120 nm. Typically, wafers etched using conventional caustic etchants exhibit a front surface 2 mm x 2 mm nanotopography of less than about 20 nm and a front surface 10 mm x 10 mm nanotopography of less than about 80 nm. A wafer etched using a caustic etchant in which the source of hydroxide ions is present at a concentration of greater than 55% by weight typically exhibits a front surface 2 mm x 2 mm nanotopography that is less than about 20 nm and, more typically, from about 10 nm to about 20 nm. A wafer etched in this manner also typically exhibits a front surface 10 mm x 10 mm nanotopography that is less than about 40 nm and, more typically, from about 25 nm to about 40 nm. Typically, a wafer etched using a caustic etchant containing one of the salt additives discussed above exhibits a front surface 2 mm x 2 mm nanotopography that is less than about 15 nm and, more typically, from about 7 nm to about 15 nm. A wafer etched in this manner also typically exhibits a front surface 10 mm x 10 mm nanotopography that is less than about 35 nm and, more typically, from about 25 nm to about 35 nm.

[00085] Silicon wafers etched with either an acidic or caustic etchant may also be characterized by the Site Flatness Least Squares Range (site flatness, or, SFQR) (SEMI M1-1296) which is the difference between a least-squares fitted plane based on a series of points within a particular site on the wafer surface having a defined size (e.g., a 20 x 20 mm site) and the actual height of the

wafer surface. The SFQR value for a particular site is determined by an ADE capacitance measurement (e.g., an ADE 9600 flatness station). A silicon wafer will have numerous 20 x 20 mm sites. For example, a silicon wafer having a diameter of 200 mm will have 52 20 x 20 mm sites and, accordingly, will have 52 SFQR measurements. Site flatness values for a particular wafer may be expressed as an average of the SFQR measurements for the sites on a wafer surface (site flatness average, or, SFQRavg) or as the maximum SFQR measurement for the wafer (site flatness maximum, or, SFQRmax). The SFQR measurements for all the sites on the wafer surface may also be used to express the overall distribution of the site flatness for a particular wafer, referred to as the "all-site" SFQR data for the wafer. SFQRavg, SFQRmax and all-site SFQR data may also be expressed in terms of the sites present on a predetermined number of wafers (e.g., a set of 100 wafers, each having 52 sites, would incorporate SFQR measurements for 5200 sites). For example, the SFQR measurements for all sites for a set of 100 wafers may be plotted and the all-site data expressed in terms of a percentage of wafer sites (X) having a site flatness below a certain value (Y).

[00086] A distinction between the flatness of the entire wafer surface (i.e., GBIR) and the flatness of a particular site on the wafer surface (i.e., SFQR) is useful because individual integrated circuits or a group of integrated circuits designed for a particular purpose placed on the wafer surface are typically approximately the size of a 20 x 20 mm site. Individual sites appropriate for incorporation of an integrated circuit generally require a certain minimum site flatness of about 0.13 μm. Thus, SFQR values may be used by device manufacturers to determine the suitability of wafers for particular applications.

[00087] In accordance with the present invention, it has been observed that in addition to improved overall flatness, the etched wafers produced by the process of the

present invention also exhibit improved front surface site flatness (i.e., have lower SFQR values) as compared to wafers etched with acidic etchants and conventional caustic etchants. Typically, a silicon wafer etched using an etchant in which the source of hydroxide ions is present at a concentration of greater than 55% by weight exhibits a front surface SFQRavg of less than about 0.13 μm. Preferably, a wafer etched in this manner will exhibit a SFQRavg of from about 0.05 μm to about 0.13 μm and, more preferably, from about 0.05 μm to about 0.08 μm. Typically, a silicon wafer etched with a caustic etchant having the source of hydroxide ions present at a concentration of greater than 55% by weight exhibits a front surface SFQRmax of less than about 0.18 μm. Preferably, a wafer etched in this manner exhibits a SFQRmax of from about 0.10 μm to about 0.18 μm and, more preferably, from about 0.10 μm to about 0.15 μm. Generally, 80% of the 20 x 20 mm sites of a wafer or group of wafers etched in this manner exhibit SFQR measurements of less than about 0.08 μm while 50% of the 20 x 20 mm sites of a wafer or group of wafers etched in this manner exhibit SFQR measurements of less than about 0.07 μm. Preferably, 80% of the 20 mm x 20 mm sites of a wafer or group of wafers etched in this manner exhibit SFQR measurements of from about 0.06 μm to about 0.08 μm and, more preferably, from about 0.06 μm to about 0.07 μm.

[00088] Typically, no more than about 20% of the sites on a wafer etched with an acidic etchant will exhibit flatness suitable for incorporation of one or more integrated circuits. Generally, no more than about 90% of the sites on a wafer etched with a conventional caustic etchant will exhibit flatness suitable for incorporation of one or more integrated circuits. While etching with conventional caustic etchants produces wafers having a much higher percentage of sites exhibiting flatness suitable for incorporation of integrated circuits, device manufacturers desire wafers with an even higher percentage of sites

suitable for incorporation of integrated circuits. In accordance with the present invention, typically at least about 99% of the sites on a wafer surface etched using a caustic etchant containing water at a concentration of less than 45% by weight exhibit flatness suitable for incorporation of one or more integrated circuits.

[00089] Thus, wafers etched in accordance with the present invention exhibit improved (i.e., reduced) SFQRavg and SFQRmax values as compared to wafers etched with acidic etchants and conventional caustic etchants over the entire wafer surface. Accordingly, more sites suitable for incorporation of one or more integrated circuits are provided.

[00090] Typically, wafers etched with acidic and caustic etchants exhibit decreased site flatness (i.e., higher SFQR values) at or near the edge of the wafer surface. This decrease in flatness at or near the edge of the wafer surface observed in wafers etched with acidic etchants and conventional caustic etchants is commonly referred to as "roll-off". In recent years, manufacturers have begun to place devices closer to the edge of the wafer surface and, since flatness of that portion of the wafer surface where a device is to be incorporated is important, the roll-off problem observed in acid etched wafers and conventional caustic etched wafers has become an important consideration of device manufacturers since it reduces the amount of the wafer surface suitable for device incorporation. Thus, in addition to improving the flatness of the overall wafer surface, it is particularly desired to improve the flatness for a given wafer at or near the edge of the wafer surface. Accordingly, SFQRavg and SFQRmax values with reference to the edge of the wafer surface or a particular region including the edge of the wafer surface are preferably minimized.

[00091] It has been observed that wafers etched with an etchant containing a source of hydroxide ions comprising sodium hydroxide and present at a concentration of greater

than 55% by weight exhibit improved site flatness (i.e., decreased SFQR values) at or near the edge of the wafer surface as compared to wafers etched with acidic etchants and conventional caustic etchants. In particular, a wafer of radius R etched in this manner generally exhibits a front surface SFQRavg of no more than about 0.13 μm in an annular region of the wafer from 2/3R measured from the central axis of the wafer to the peripheral edge of the wafer. Typically, a wafer etched in this manner exhibits a front surface SFQRavg of from about 0.05 μm to about 0.13 μm in such an annular region. In addition, a wafer etched in this manner generally exhibits a front surface SFQRmax of no more than about 0.18 μm in an annular region of the wafer from 2/3R measured from the central axis of the wafer to the peripheral edge of the wafer. Typically, a wafer etched in this manner exhibits a front surface SFQRmax of from about 0.05 μm to about 0.18 μm in such an annular region. Thus, wafers etched in this manner typically possess a greater number of sites near the edge of the wafer surface exhibiting flatness suitable for incorporation of one or more integrated circuits.

[00092] With respect to backside morphology, a wafer etched in accordance with the present invention exhibits suitable characteristics either as-etched or after having been subjected to one or more further operations (i.e., polishing). Generally, a wafer etched in accordance with the present invention exhibits an average back surface roughness of less than about 0.30 μm Ra. Preferably, a wafer etched using a caustic etchant containing a source of hydroxide ions at a concentration of greater than 55% by weight exhibits an average back surface roughness of from about 0.15 μm to about 0.25 μm Ra, more preferably from about 0.22 μm to about 0.25 μm Ra and, still more preferably, from about 0.22 μm to about 0.23 μm Ra. Generally, a wafer etched in this manner exhibits a maximum back surface roughness of less than about 3.0 μm Rmax. Preferably, the wafer exhibits a maximum back surface

roughness of from about 2.2 μm to about 2.8 μm Rmax, more preferably from about 2.2 μm to about 2.5 μm Rmax and, still more preferably, from about 2.2 μm to about 2.3 μm Rmax.

[00093] Generally, a wafer etched in accordance with the present invention using a caustic etchant containing one of the salt additives discussed above exhibits an average back surface roughness of less than about 0.20 μm Ra. Preferably, a wafer etched in this manner exhibits an average back surface roughness of from about 0.12 μm to about 0.20 μm Ra. Generally, a wafer etched in this manner exhibits a maximum back surface roughness of less than about 2.0 μm Rmax. Preferably, the wafer will exhibit a maximum back surface roughness of from about 1.2 μm to about 2.0 μm Rmax.

[00094] Generally, the back surface of a wafer etched using a caustic etchant containing a source of hydroxide ions at a concentration of greater than 55% by weight has a reflectance of less than about 100 gloss units. Typically, in the case of a caustic etchant comprising potassium hydroxide, the etched wafer has a reflectance of from about 20 to about 50 gloss units. When the caustic etchant comprises sodium hydroxide, the etched wafer typically has a reflectance of from about 80 to about 100 gloss units. Generally, the back surface of a wafer etched using a caustic etchant containing one of the salt additives discussed above exhibits a back surface reflectance that is at least about 80 gloss units and, more typically, from about 80 to about 160 gloss units. In particular, when the salt additive includes potassium fluoride the etched wafer typically has a reflectance of from about 70 to about 90 gloss units. When the salt additive includes potassium carbonate, the etched wafer typically has a reflectance of from about 140 to about 160 gloss units.

[00095] In a preferred embodiment in which a wafer is etched using the caustic etchant of the present invention

containing one of the salt additives discussed above, the wafer exhibits a flatness that is less than about 0.5 μm, a front surface 2 mm x 2 mm nanotopography that is less than about 7 nm, a front surface 10 mm x 10 mm nanotopography that is less than about 25 nm, an average back surface roughness of less than about 0.12 μm Ra and a maximum back surface roughness of less than about 1.2 μm Rmax, and a back surface reflectance that is at least about 80 gloss units.

[00096] Thus, the caustic etchant of the present invention produces wafers with improved overall flatness (including site flatness) as compared to acid etched wafers and may further produce wafers with improved overall flatness (including site flatness) as compared to wafers etched with conventional caustic etchants. Also, when wafers are etched in accordance with the present invention utilizing sodium hydroxide as the source of hydroxide ions, improved flatness at or near the edge of the wafer surface, as compared to both acid etched wafers and wafers etched with conventional caustic etchants has been observed. In addition, the caustic etchant of the present invention produces wafers which exhibit a decreased surface roughness compared to wafers etched with conventional caustic etchants.

[00097] After etching, the wafer is typically subjected to a polishing operation to reduce the surface roughness of the wafer to a level acceptable for semiconductor device manufacturers (e.g., from about 0.02 nm to about 0.5 nm based upon Atomic Force Microscopy of a 10 μm x 10 μm field of view). The improved surface characteristics exhibited by the etched wafers of the present invention result in reduced polishing time as compared to those produced with conventional caustic etchants. The polishing operation is conducted using conventional apparatus and materials known to those skilled in the art. Generally, the back surface of a wafer etched in accordance with the present invention which has been

subjected to a polishing operation may have a reflectance of up to about 300 gloss units. Typically, the back surface of a wafer etched in accordance with the present invention which has been subjected to a polishing operation will be from about 120 gloss units to about 300 gloss units and, more typically, from about 140 gloss units to about 180 gloss units. In a preferred embodiment, the wafer etched according to the present invention is subjected to a double side polishing operation wherein the front and back sides of the wafer are polished concurrently. Methods for double side polishing are known in the art, including those found, for example, in U.S. Patent Nos. 5,110,428; 5,422,316; 5,952,242; 5,963,821; 6,043,156; 6,051,498; 6,162,730; 6,189,546; and 6,376,335, the entire disclosures of which are hereby incorporated by reference. The polishing operation results in a wafer exhibiting a specular (i.e., mirror-like) appearance.

[00098] In a preferred embodiment the wafer produced in accordance with the present invention exhibits, after polishing, a front surface SFQRavg of less than about 0.13 μm, a front surface SFQRmax of less than about 0.18, a front surface 2 mm x 2 mm nanotopography of less than about 20 nm, and a front surface 10 mm x 10 mm nanotopography of less than about 40 nm. The wafer produced may also preferably exhibit an average back surface roughness of less than about 0.25 μm Ra and a maximum back surface roughness of less than about 2.5 μm Rmax, and a back surface reflectance that of less than about 180 gloss units.

[00099] In another preferred embodiment, the wafer etched according to the present invention is subjected to an operation wherein the front side of the wafer is polished while the back side of the wafer is buffed. Buffing operations are conducted using the same equipment and materials used in wafer polishing operations, but are carried out using reduced pressure applied to the wafer and/or for a shorter period of time as compared to

polishing such that considerably less stock is removed from the wafer surface than is removed during polishing. Typically, the backside of a wafer subjected to the buffing operation has an average surface roughness that is reduced to less than about 0.18 μm Ra and a reflectance of at least about 150 gloss units (per ASTM D 523, ISO 2813 or DIN 67530 standards with an angle of incidence of 60°).

[000100] In another embodiment the wafer is concurrently etched with the caustic etchant of the present invention while being polished. This embodiment is carried out by injecting the caustic etchant between the wafer and one or more of the pads used to polish the wafer. Suitable polishing apparatus include the AC 1500 P or the AC 2000 P double sided polisher, both commercially available from Peter Wolters AG (Rendsburg, Germany), utilizing H2 or MH pads commercially available from Rodel (Scottsdale, AZ), or Fujikoshi (Japan), or SpeedFam-IPEC (Des Plaines, IL).

[000101] Polishing increases the total thickness variation of the wafer by about 0.1 μm to about 1.5 μm (e.g., current detection limits are about 0.01 μm, for conventional capacitance measuring devices such as the ADE 7200 or ADE 9600) and deposits contaminants such as particulate matter (e.g., silica polishing media), foreign metals (e.g., iron, zinc and aluminum), and organic compounds on the wafer surface. For example, a typical polished 200 mm wafer is estimated to have approximately 1 to 3 million particles exceeding about 0.2 μm in diameter on the surface. The foregoing particle count is an estimate because the extent of particle contamination after polishing is so great that conventional laser scanning counting devices such as the Tencor (San Jose, CA) 6200, Tencor SP1, ADE CR80 or ADE CR81 cannot accurately determine counts above about 20,000 particles per wafer. A typical polished wafer also has about 1×10^{15} metal atoms/cm^2 (as determined, for example, by Acid Drop Inductive Coupled Plasma Mass Spectroscopy), and at least about 5×10^{15} organic carbon atoms/cm^2 (determined, for

example, by Gas Chromatography/Atomic Emission Spectroscopy).

[000102] Current specifications for a Grade 1 wafer typically require that the concentration of contaminant particles exceeding 0.2 μm in diameter adsorbed to the wafer surface be no greater than about 0.06 to about 0.16 particles/cm^2 (e.g., the front of a 200 mm diameter Grade 1 wafer has no more than about 50 particles exceeding about 0.2 μm in diameter); that there be no more than about 1 x 10^{10} metal atoms/cm^2; and that there be no more than about 1 x 10^{14} organic carbon atoms/cm^2. To achieve these target concentrations, therefore, the wafer must be subjected to a cleaning method after polishing. Numerous cleaning methods are known in the art to reduce the concentration of surface contaminants (e.g., RCA cleaning, Piranha-RCA cleaning, megascopic and ultrasonic cleaning, scrubbing and acid etching).

[000103] To adequately clean the surface of a polished silicon wafer such that it is substantially free of contaminants (i.e., contamination no greater than the levels corresponding to a Grade 1 wafer), conventional manufacturing methods typically involve at least two cleaning operations after final polishing: a first post-polish cleaning operation followed by a final cleaning operation with the wafer being dried as the last step of a post-polish cleaning operation. During a post-polish cleaning operation which may, for example, comprise 10 or more steps (e.g., alkaline cleaning steps such as SC-1, acid cleaning steps such as hydrofluoric acid or SC-2, deionized water rinsing steps, and drying steps), the particle count on the front surface of a polished 200 mm wafer may be reduced to about 50 particles exceeding about 0.2 μm in diameter. During a final cleaning operation which may, for example, comprise another 10 or more steps (e.g., alkaline cleaning steps such as SC-1, acid cleaning steps such as hydrofluoric acid or SC-2, deionized water rinsing steps, and drying steps), the particle count on the

front surface of a polished 200 mm wafer may be further reduced to about 15 or fewer particles exceeding about 0.2 μm in diameter.

[000104] The present invention is illustrated by the following examples which are merely for the purpose of illustration and not to be regarded as limiting the scope of the invention or manner in which it may be practiced.

[000105] **EXAMPLE 1**

[000106] This example demonstrates the use of a caustic etchant which comprises sodium hydroxide as the source of hydroxide ions at a concentration of approximately 58% by weight. This example also compares wafers etched in accordance with the present example with data for wafers etched using a conventional caustic etchant containing 50% by weight sodium hydroxide.

[000107] The caustic etchant was prepared by mixing 26.5 kg of sodium hydroxide with 120 l of a 50% by weight sodium hydroxide solution to produce a caustic etchant containing approximately 58% by weight of sodium hydroxide.

[000108] 360 200 mm diameter P^+ silicon wafers were etched over the course of 15 etching runs in an etch tank having a capacity of approximately 100 l through which the caustic etchant prepared as described above was continuously circulated during etching. The wafers to be etched were placed in cassettes able to hold 25 wafers and the wafers were immersed in the caustic etchant by placing the cassette of wafers into a driven, rotatable basket which was submerged in the etchant. The temperature of the caustic etchant was maintained at about 80°C. During each of the 15 etching runs, the wafers remained immersed in the etchant for from about 7 minutes to about 9 minutes which was a sufficient period of time to remove approximately 23 μm of silicon from the surface of each of the wafers. Silicon removal measurements were made using an ADE 9500 capacitance gauge manufactured by ADE Semiconductor, Inc. (Westwood, MA). In the present example, the measurement was made with the gauge set at a 2mm edge exclusion. Over

the course of the 15 etching runs, the etching removal rate ranged from about 2.55 μm/minute to about 3.28 μm/minute.

[000109] The surface of the etched silicon wafers exhibited facets having both a length and width of approximately 7 μm, compared to wafers etched using a conventional caustic etchant containing 50% by weight sodium hydroxide and etched in accordance with the procedure set forth above which exhibit facets having both a length and width of approximately 12 μm. The dimensions of the facets of the etched wafers were measured using an Olympus, BH3 Microscope at 200X magnification. Wafers etched using a conventional caustic etchant containing approximately 45% by weight potassium hydroxide and in accordance with the procedure set forth above typically exhibit facets having a length and width of approximately 18 μm. Fig. 1 and Fig. 2 are photomicrographs of wafers etched in accordance with the present example using the caustic etchant containing approximately 58% by weight sodium hydroxide produced using the Olympus, BH3 Microscope at 200X magnification described above for measuring the dimensions of the facets on the surface of the etched wafers.

[000110] Fig. 3 depicts the range of gloss measurements of the 360 200 mm P^+ wafers etched during the 15 etching runs. As shown, the gloss of the wafers after etching and polishing ranged from approximately 155 gloss units to approximately 190 gloss units. Gloss measurements appearing throughout these examples were made using a BYK-Gardner mirror-TRI-gloss gloss meter (0-2000 gloss units, GB-4050) manufactured by BYK-Gardner, USA (Columbia, MD) in accordance with ASTM D 2457 D 523, ISO 2813 or DIN 67530.

[000111] **EXAMPLE 2**

[000112] This example further demonstrates the use of a caustic etchant comprising sodium hydroxide as the source of hydroxide ions prepared in accordance with the procedure described in Example 1 and containing approximately 58% by weight sodium hydroxide.

[000113] 365 200 mm diameter P^- silicon wafers were etched as described above in Example 1 over the course of 20 etching runs. Over the course of the 20 etching runs, the etching removal rate ranged from about 2.5 μm/minute to about 3.8 μm/minute.

[000114] Fig. 4 shows the GBIR of the wafers before and after etching. GBIR measurements appearing throughout these examples were made using an ADE 9500 capacitance gauge manufactured by ADE Semiconductor, Inc. (Westwood, MA). In the present example, the capacitance gauge was set at a 3 mm edge exclusion. As shown, the etched silicon wafers exhibited an improved overall flatness, or, GBIR, after etching. For example, approximately 50% of the wafers exhibited a GBIR at or below about 0.80 μm prior to etching and approximately 50% of the wafers exhibited a GBIR at or below about 0.60 μm after etching. By comparison, wafers etched using a conventional caustic etchant containing approximately 50% by weight sodium hydroxide do not exhibit improved flatness after etching as compared to flatness after lapping (i.e., approximately 50% of wafers exhibiting a GBIR at or below about 0.8 μm after lapping and prior to etching with a conventional caustic etchant in accordance with the procedure set forth above will exhibit a GBIR at or below about 0.8 μm after etching).

[000115] Fig. 5 shows SFQRmax measurements of the wafers both before and after etching. SFQRmax measurements appearing throughout these examples were made using the ADE 9500 capacitance gauge manufactured by ADE Semiconductor, Inc. (Westwood, MA) described above and used for the GBIR measurements. The capacitance gauge was also set at a 3 mm edge exclusion for the SFQRmax measurements. As shown, a majority of the wafers etched with the caustic etchant containing approximately 58% by weight sodium hydroxide exhibited improved front surface SFQRmax. For example, approximately 50% of the wafers exhibited an SFQRmax at or below about 0.14 μm prior to etching and an SFQRmax at or

below about 0.13 μm after etching. By comparison, approximately 50% of wafers exhibiting an SFQRmax at or below about 0.14 μm prior to etching and etched using a conventional caustic etchant containing approximately 50% by weight sodium hydroxide in accordance with the procedure set forth above will exhibit an SFQRmax at or below about 0.15 after etching.

[000116] Fig. 6 shows gloss and average surface roughness measurements for the 365 wafers etched during the course of the 20 etching runs. Surface roughness measurements appearing throughout these examples were made using a Federal Gage Surfanalyzer 5000 (Federal Products Surface Analyzer 5000) manufactured by the former Federal Products, Inc., now known as Mahr Federal, Inc. (Providence, RI). As shown in Fig. 6, the etched wafers exhibited an average surface roughness of from about 0.16 μm Ra to about 0.21 μm Ra after etching and polishing. As etched, the average surface roughness of the wafers ranged from about 0.25 to about 0.32 μm Ra. Also shown in Fig. 6, the etched wafers exhibited a reflectance ranging from about 27 gloss units to about 45 gloss units.

[000117] **EXAMPLE 3**

[000118] This example further demonstrates the use of a caustic etchant comprising sodium hydroxide as the source of hydroxide ions prepared in accordance with the procedure described in Example 1 and containing approximately 58% by weight sodium hydroxide.

[000119] In order to compare the performance of different abrasives, prior to lapping the wafers were divided into two groups: Group 1 consisting of 1551 wafers which were lapped with PWA 9 abrasive manufactured by Fujimi America, Inc. (Wilsonville, OR) and Group 2 consisting of 100 wafers which were lapped using FO 1200 abrasive also manufactured by Fujimi America, Inc. (Wilsonville, OR).

[000120] The 1651 200 mm diameter P^- silicon wafers were etched as described above in Example 1 over the course

of 83 etching runs (78 runs for etching of the Group 1 wafers and 5 runs for etching the Group 2 wafers) with the cassette generally containing 20 wafers for each etching run, however, for the 77th run the cassette contained 16 wafers and for the 78th run the cassette contained 15 wafers. As shown in Fig. 7, over the course of the 83 etching runs, the etching removal rate ranged from about 3.2 μm/minute to about 3.8 μm/minute.

[000121] Fig. 8 shows GBIR values for lapped wafers and for the wafers etched in accordance with the present example. As shown, the silicon wafers exhibited an improved overall flatness, or, GBIR, after etching. For example, approximately 50% of the wafers exhibited a GBIR at or below about 0.85 μm after lapping but prior to etching and approximately 50% of the wafers exhibited a GBIR at or below about 0.65 μm after etching. By comparison, wafers etched using a conventional caustic etchant containing approximately 50% by weight sodium hydroxide do not exhibit improved flatness after etching as compared to flatness after lapping (i.e., in the case of wafers etched using a conventional caustic etchant, when approximately 50% of wafers lapped in accordance with the above method exhibit a GBIR at or below about 0.85 μm after lapping, after etching with a conventional caustic etchant in accordance with the procedure set forth above approximately 50% of wafers exhibit a GBIR at or below about 0.85 μm).

[000122] Fig. 9 shows SFQRmax values on 25 mm x 25 mm sites for wafers of Group 1 lapped and etched in accordance with the present example. The capacitance gauge described in Examples 1 and 2 was set at a 2 mm edge exclusion for the GBIR and SFQRmax measurements. As shown, certain of the etched silicon wafers exhibited improved front surface SFQRmax. For example, approximately 50% of the wafers exhibited an SFQRmax at or below about 0.20 μm after lapping and prior to etching and approximately 50% of the wafers exhibited an SFQRmax at or below about 0.17 μm after

etching. By comparison, approximately 43% of wafers lapped in accordance with the above method and etched using a conventional caustic etchant containing approximately 50% by weight sodium hydroxide and in accordance with the procedure set forth above exhibit an SFQRmax at or below about 0.17 μm.

[000123] Figs. 10, 11 and 12 are photomicrographs of wafers from Group 1 etched during different runs produced using an Olympus, BH3 Microscope at 200X magnification. Fig. 10 depicts a wafer etched during etching run 23 during which 21.1 μm of silicon was removed from the wafer surface to produce a wafer having a gloss of approximately 29 gloss units and an average surface roughness of approximately 0.242 μm Ra. Fig. 11 depicts a wafer etched during etching run 50 during which 20.7 μm of silicon was removed from the wafer surface to produce a wafer having a gloss of approximately 28 gloss units and an average surface roughness of approximately 0.226 μm Ra. Fig. 12 depicts a wafer etched during etching run 70 during which 21.6 μm of silicon was removed from the wafer surface to produce a wafer having a gloss of approximately 33 gloss units and an average surface roughness of approximately 0.244 μm Ra. The gloss and roughness measurements were made as described in Examples 1 and 2, respectively.

[000124] Fig. 13 is a photomicrograph of a wafer from Group 2 etched during one of the final 5 etching runs (79-83) runs produced using an Olympus, BH3 Microscope at 200X magnification. Fig. 13 depicts a wafer etched such that 17.4 μm of silicon was removed from the wafer surface to produce a wafer having a gloss of approximately 30 gloss units and an average surface roughness of approximately 0.172 μm Ra. The gloss and roughness measurements were made as described in Examples 1 and 2, respectively.

[000125] The average surface roughness of the wafers of Group 1 after etching ranged from about 0.22 μm Ra to about 0.25 μm Ra and the average gloss measurement was approximately 30 gloss units. The wafer of Group 2

measured and shown in Fig. 13 exhibited a surface roughness of about 0.172 μm Ra and a reflectance of approximately 30 gloss units. Thus, the etched wafers exhibited improved surface roughness overall as compared to wafers lapped in accordance with the above procedure and etched using a conventional caustic etchant containing approximately 50% by weight sodium hydroxide (wafers etched using conventional caustic etchants typically exhibit an average surface roughness of from about 0.27 μm Ra to about 0.35 μm Ra). The surface roughness measurements for the wafers of Group 1 and 2 as etched further indicate improved surface roughness as compared to wafers etched using conventional caustic etchants containing approximately 50% by weight sodium hydroxide over the course of multiple etching runs. These results also indicate the effectiveness of a caustic etchant of the present invention at providing etched wafers having desired surface characteristics under these conditions when various lapping abrasives are used.

[000126] **EXAMPLE 4**

[000127] This example further demonstrates the use of a caustic etchant containing approximately 58% by weight sodium hydroxide and prepared in accordance with the procedure described in Example 1. This example also compares wafers etched using such a caustic etchant with wafers etched using a conventional caustic etchant containing approximately 45% by weight potassium hydroxide and with data for wafers etched in accordance with a standard acidic etching protocol.

[000128] 285 200 mm diameter P^+ silicon wafers were etched as described above in Example 1 over the course of 15 etching runs. Over the course of the 15 etching runs, the etching removal rate ranged from about 2.5 μm/minute to about 3.8 μm/minute.

[000129] After etching, the wafers were polished in accordance with a differential double-side polishing process utilizing a Peter Wolters AC 1400P polisher manufactured by Peter Wolters AG (Rendsburg, Germany) in

which 15 wafers at a time were polished. Approximately 0.15 μm to about 0.20 μm of silicon was removed from the backside of each of the etched wafers during the double-side polishing process while approximately 1.5 μm of silicon were removed from the front side of the etched wafer. The double-side polished wafers exhibited improved all-site SFQR (a measure of the SFQR for all sites on each of the wafers etched) as compared to the all-site SFQR values for the as-etched wafers. All-site SFQR measurements appearing throughout these examples were made using an ADE 9700 capacitance gauge manufactured by ADE Semiconductor, Inc. (Westwood, MA). In the present example, the capacitance gauge was set at a 2 mm edge exclusion for the all-site SFQR measurements.

[000130] Fig. 14 shows SFQRmax values after lapping, after etching, and after buffing for the wafers etched using a sodium hydroxide caustic etchant of the present invention containing approximately 58% by weight prepared as described above. As shown, after etching, approximately 50% of the wafers exhibited an SFQRmax of at or below about 0.12 μm. Fig. 14 also shows that approximately 50% of the buffed wafers etched using the sodium hydroxide caustic etchant of the present invention exhibited an SFQRmax of at or below about 0.10 μm.

[000131] Fig. 15 shows SFQRmax values after lapping, after etching, and after buffing for the wafers etched using the standard caustic etchant containing approximately 45% by weight potassium hydroxide. As shown, after etching approximately 50% of the wafers etched using the standard potassium hydroxide caustic etchant containing approximately 45% by weight potassium hydroxide exhibited an SFQRmax of at or below about 0.17 μm. Fig. 15 also shows that approximately 50% of the buffed wafers etched using the standard potassium hydroxide caustic etchant containing approximately 45% by weight potassium hydroxide exhibited an SFQRmax of at or below about 0.14 μm.

[000132] Fig. 16 shows SFQRmax values for wafers etched using the caustic etchant prepared as described above containing approximately 58% by weight sodium hydroxide and wafers etched using a standard potassium hydroxide caustic etchant containing approximately 45% by weight potassium hydroxide, before and after polishing. The capacitance gauge was set at an edge exclusion of 2 mm for the SFQRmax measurements.

[000133] As shown in Fig. 16, approximately 50% of the wafers etched using the sodium hydroxide caustic etchant of the present invention containing approximately 58% by weight sodium hydroxide exhibit an SFQRmax before polishing of at or below about 0.115 μm. Also shown in Fig. 16, approximately 50% of the wafers etched using the standard potassium hydroxide caustic etchant containing approximately 45% by weight potassium hydroxide exhibit an SFQRmax before polishing of at or below about 0.145 μm. Also shown in Fig. 16, approximately 50% of the wafers etched using the sodium hydroxide caustic etchant of the present invention containing approximately 58% by weight sodium hydroxide exhibit an SFQRmax after polishing of at or below about 0.10 μm. Further shown in Fig. 16, approximately 50% of the wafers etched using the standard potassium hydroxide caustic etchant containing approximately 45% by weight potassium hydroxide exhibit an SFQRmax after polishing of at or below about 0.11 μm.

[000134] The all-site SFQR values for the lapped, etched and polished wafers of the present example were compared to wafers etched with a standard potassium hydroxide caustic etchant. The potassium hydroxide caustic etchant used for comparison purposes consisted of 120 l of a standard 45% by weight potassium hydroxide solution. 200 200 mm diameter P^+ silicon wafers were etched with the standard potassium hydroxide caustic etchant over the course of 8 etching runs in accordance with the etching process described above in Example 1 except the temperature of the standard 45% by weight potassium hydroxide etchant

was maintained at about 90°C. The wafers etched using the standard 45% by weight potassium hydroxide etchant were polished in accordance with the above description in the present example.

[000135] Fig. 17 shows all-site SFQR values for wafers etched using the sodium hydroxide caustic etchant of the present invention containing approximately 58% by weight sodium hydroxide and for wafers etched using a standard potassium hydroxide caustic etchant containing approximately 45% by weight potassium hydroxide, before and after polishing. The capacitance gauge was set at an edge exclusion of 2 mm for the all-site SFQR measurements.

[000136] As shown in Fig. 17, approximately 50% of the wafers etched using the sodium hydroxide caustic etchant of the present invention containing approximately 58% by weight sodium hydroxide exhibit an all-site SFQR before polishing of at or below about 0.045 μm. Also shown in Fig. 17, approximately 50% of the wafers etched using the standard potassium hydroxide caustic etchant containing approximately 45% by weight potassium hydroxide exhibit an all-site SFQR before polishing of at or below about 0.065 μm.

[000137] Further shown in Fig. 17, approximately 50% of the wafers etched using the sodium hydroxide caustic etchant of the present invention containing approximately 58% by weight sodium hydroxide exhibit an all-site SFQR after polishing of at or below about 0.05 μm and approximately 50% of the wafers etched using the standard potassium hydroxide caustic etchant containing approximately 45% by weight potassium hydroxide exhibit an all-site SFQR after polishing of at or below about 0.054 μm.

[000138] For further comparison purposes, Fig. 18 shows all-site SFQR data for wafers etched using an acidic etchant containing hydrofluoric acid (HF), nitric acid (HNO_3) and phosphoric acid (H_3PO_4) in accordance with the procedure set forth in U.S. Patent No. 5,340,437 using a

vertical etcher formerly manufactured by Steag AG (Donaueschegen, Germany), now manufactured by Santa Clara Plastics (Boise, ID). In accordance with the procedure of U.S. Patent No. 5,340,437, the etch time is approximately 2.5 minutes, the etching temperature is approximately 35°C and approximately 23 μm of silicon is removed from the surface of the wafer. As shown in Fig. 18, approximately 50% of wafers etched in accordance with this standard etching protocol will exhibit an all-site SFQR at or below about 0.27 μm.

[000139] Thus, wafers etched using a caustic etchant containing sodium hydroxide at a concentration of approximately 58% by weight exhibit advantageous surface characteristics as characterized by all-site SFQR measurements compared to wafers etched using a standard potassium hydroxide caustic etchant containing approximately 45% by weight potassium hydroxide and wafers etched using a conventional acidic etchant in a standard acidic etching protocol.

[000140] Thus, wafers etched in accordance with the above methods using the high concentration sodium hydroxide caustic etchant exhibit improved surface characteristics characterized by reduced SFQRmax and all-site SFQR values compared to wafers etched in accordance with the above methods using a conventional potassium hydroxide caustic etchant.

[000141] **EXAMPLE 5**

[000142] This example demonstrates the use of a caustic etchant which includes a salt additive comprising potassium fluoride.

[000143] A 1:1 molar ratio solution of anhydrous potassium fluoride (220 g) in water (70g) was first prepared. The caustic etchant was prepared by mixing this solution with a 45% by weight aqueous solution of potassium hydroxide (300 g). This produced a caustic etchant comprising about 35 mole percent potassium hydroxide, about

22 mole percent potassium fluoride and about 43 mole percent water.

[000144] A 25 mm x 75 mm P+ silicon wafer specimen was held by teflon tweezers and immersed in the caustic etchant prepared in accordance with the method set forth above (approximately 100 ml) and contained in a 120 ml beaker. The temperature of the etchant was maintained at about 80°C. The caustic etchant was agitated by a magnetic stirring bar to promote contact between the wafer specimen and the etchant and to promote a more uniform etchant temperature.

[000145] After immersion for approximately 8 minutes and 15 seconds, during which time 18.8 μm of silicon was removed from the surface of the wafer specimen, the silicon specimen was withdrawn from the etchant. Silicon removal measurements for the present example were made using an ADE Microsense 6033 capacitance gauge manufactured by ADE Semiconductor, Inc. (Westwood, MA).

[000146] The etched silicon wafer specimen exhibited facets having both a length and width of approximately 20 μm, similar in size to those exhibited by wafers etched using caustic etchants which do not contain a salt additive. The dimensions of the facets of the etched wafers were measured using an Olympus, BH3 Microscope at 1000X magnification. However, the facets of the wafer specimen etched using a caustic etchant containing a salt additive are more rounded than those typically exhibited by wafers etched with caustic etchants which do not contain a salt additive. Fig. 19 is a photomicrograph of the etched wafer specimen produced using an Olympus, BH3 Microscope at 1000X magnification depicting the size and character of the facets of the wafer specimen etched in the present example.

[000147] The gloss of the wafer specimen was approximately 83 gloss units, as compared to wafers etched using caustic etchants which do not contain a salt additive which typically exhibit gloss measurements of from about 90 to about 120. The average surface roughness of the wafer

specimen etched in the present example was about 0.39 μm Ra.

[000148] **EXAMPLE 6**

[000149] This example demonstrates the use of a caustic etchant which includes a salt additive comprising potassium carbonate.

[000150] The caustic etchant was prepared by mixing 75.4 g of potassium carbonate, 75.1 g of water and 15.1 g of a 45 wt% aqueous potassium hydroxide solution. This produced a caustic etchant comprising about 11 mole percent (10 wt%) potassium hydroxide, about 6 mole percent (45 wt%) potassium carbonate and about 83 mole percent (45 wt%) of water.

[000151] A 25 mm x 75 mm P+ silicon wafer specimen was held by teflon tweezers and immersed in the caustic etchant prepared in accordance with the method set forth above (approximately 100 ml) and contained in a 120 ml beaker. The temperature of the etchant was maintained at about 100°C. The caustic etchant was agitated by a magnetic stirring bar to promote contact between the wafer specimen and the etchant and to promote a more uniform etchant temperature.

[000152] After immersion for about 2 minutes, during which time 32.1 μm of silicon was removed from the surface of the wafer specimen, the specimen was withdrawn from the etchant. Silicon removal measurements were carried out as described above in Example 5.

[000153] The etched silicon wafer specimen exhibited facets having both a length and width of approximately 20 μm, similar in size to facets exhibited by wafers etched using caustic etchants which do not contain a salt additive. The dimensions of the facets of the etched wafers were measured using an Olympus, BH3 Microscope at 200X magnification. However, the facets of the wafer specimen etched using a caustic etchant containing a salt additive are more rounded than those typically exhibited by wafers subjected to conventional caustic etching in the

absence of a salt additive. Fig. 20 is a photomicrograph of the etched wafer specimen produced using an Olympus, BH3 Microscope at 200X magnification depicting the size and character of the facets of the wafer specimen etched in the present example.

[000154] The gloss of the wafer specimen was about 140 gloss units while the average surface roughness of the wafer specimen was about 0.23 μm Ra.

[000155] For comparison purposes, a wafer was etched in accordance with the procedure described above in Example 1 using a conventional caustic etchant containing approximately 45% by weight potassium hydroxide which did not contain a salt additive. The temperature of the etchant was maintained at about 90°C. The wafer remained in contact with the etchant for from about 7 to about 9 minutes during which time from about 20 to 25 μm of silicon was removed from the surface of the wafer. Silicon removal measurements were carried out as described above in Example 5. The wafer etched using the caustic etchant containing approximately 45% by weight potassium hydroxide but no salt additive exhibited a reflectance of between about 90 and about 110 gloss units and an average surface roughness of about 0.3 μm Ra. Thus, the wafer specimen etched as described in the present example using a caustic etchant containing a salt additive exhibits improved surface characteristics compared to wafers etched using caustic etchants which do not contain a salt additive.

[000156] The present invention is not limited to the above embodiments and can be variously modified. The above description of preferred embodiments is intended only to acquaint others skilled in the art with the invention, its principles and its practical application so that others skilled in the art may adapt and apply the invention in its numerous forms, as may be best suited to the requirements of a particular use.

[000157] With reference to the use of the word(s) "comprise" or "comprises" or "comprising" in this entire

specification (including the claims below), it is noted that unless the context requires otherwise, those words are used on the basis and clear understanding that they are to be interpreted inclusively, rather than exclusively, and that it is intended each of those words to be so interpreted in construing this entire specification.